CLAIMS

What is claimed is:

1. An application specific integrated circuit (ASIC) comprising:

a standard cell, the standard cell including a plurality of logic functions; and

at least one FPGA interconnect coupled to the plurality of functions, wherein the at least one FPGA interconnect can be configured to select one of the plurality of logic functions.

2. The ASIC of claim 1 wherein the one logic function is coupled to a plurality of I/O pins by the at least one configured FPGA interconnect.

3. The ASIC of claim 1 wherein the one logic function is coupled to an internal bus via the at least one configured FPGA interconnect.

4. An application specific integrated circuit (ASIC) comprising:

a standard cell, the standard cell including a plurality of logic functions;

a plurality of input output (I/O) pins; and

at least one field programmable gate array (FPGA) interconnect coupled the plurality of I/O pins and the plurality of logic functions, wherein the at least one FPGA interconnect can be configured to select one of the plurality of logic functions utilizing field programming techniques.

5. The ASIC of claim 4 wherein the one logic function is coupled to an internal bus via the at least one configured FPGA interconnect.

6. An application specific integrated circuit (ASIC) comprising:

a standard cell, the standard cell including a plurality of logic functions;

a at least one internal bus; and

at least one field programmable gate array (FPGA) interconnect coupled to at least one internal bus and the plurality of logic functions, wherein the at least one FPGA interconnect can be configured to select one of the plurality of logic functions utilizing field programming techniques.

7. The ASIC of claim 6 wherein the one logic function is coupled to a plurality of I/O pins by the at least one configured FPGA interconnect.

8. An application specific integrated circuit (ASIC) comprising:

a standard cell, the standard cell including a plurality of logic functions;

at least one bus coupled to the plurality of functions;

a plurality of I/O pins; and

at least one FPGA interconnect coupled between the at least one bus and the plurality of I/O pins, wherein the at least one FPGA interconnect can be utilized to correct wiring error when the ASIC is utilized on a printed circuit board.

9. The ASIC of claim 8 wherein the wiring error is a reversed bit order wiring

error.

10. An application specific integrated circuit (ASIC) comprising:

a plurality of I/O pins;

a plurality of first logic functions;

a first field programmable gate array (FPGA) interconnect coupled between the plurality of I/O pins and the plurality of first logic function, wherein the first FPGA interconnect can be configured to select at least one of the plurality of first logic functions;

a bus coupled to a plurality of first logic functions; and

a second FPGA interconnect coupled between the bus and the plurality of first logic functions, wherein the second FPGA interconnect is configured to connect to one of the plurality of first logic functions to the bus.

11. The ASIC of claim 10 which includes a plurality of second logic functions coupled to the bus.